REMARKS

The Examiner's action dated June 24, 2004, has been received, and its contents carefully noted.

In response to the objection to the Specification, presented in section 1 of the Action, the change suggested by the Examiner has been made.

In response to the objection to the drawings presented in section 2 of the Action, submitted herewith is a replacement sheet in which the reference numerals described on page 8 of the Specification have been provided.

In response to the claim objections presented in section 3 of the Action, all of the claims have been reviewed and amended to eliminate the informalities perceived by the Examiner. In many cases, the amendments differ from those suggested by the Examiner, but are in a form that conforms to proper English usage.

The rejection of claims 1, 3-5 and 7, presented in section 5 of the Action, is traversed for the reason that the novel printed circuit board defined in these claims, and particularly in claim 1, is not disclosed in the applied reference.

The printed circuit board defined in claim 1 of the present Application is composed of a substrate made of a material including a first resin, having a conductive pattern

thereon disposed on the top surface of the substrate, the conductive pattern having an unsheltered portion and a sheltered portion. The unsheltered portion has a base and a tip. The printed circuit board further includes a solder mask made of a resin having a thermal expansion coefficient substantially identical to that of the substrate resin. The solder mask is coated on the top surface of the substrate to form, on the top surface, a layer having a first area and a second area. The first area covers the sheltered portion and has a first thickness, while the second area, which has a thickness less than that of the first area, surrounds the base of the unsheltered portion of the conductive pattern so that the tip of that unsheltered portion is exposed.

As can be seen in Figure 6, second area 406 of solder mask 40 surrounds base 265 of unsheltered portion 263, while leaving tip 266 exposed.

In support of the rejection of this claim, the Examiner has relied on the embodiment shown in Figures 5-9 of the Reed. This embodiment differs in a number of significant respects from the printed circuit board defined in claim 1 of the present Application. It is noted that Figure 5-8 of the reference illustrate intermediate stages in the fabrication of a circuit board, and that only Figure 9 illustrates the

finished board. Reference will therefore be made herein to the structure shown in Figure 9.

According to a first feature of the invention as defined in claim 1, there is a first solder mask coated on the top surface of the substrate to form a first area having a first thickness and covering a sheltered portion of a conductive pattern, and a second area having a second thickness less than that of the first area and surrounding the base of the unsheltered portion of the conductive pattern. In the printed circuit board shown in Figure 9 of the reference, there is only one layer that is identified as a solder mask, which is layer 90. It is noted, however, that layer 62 may be a screen stencil printed solder mask composition. Layer 68 is a photo-resist film and there is no evidence that this photo-resist film will be constituted by a resin.

In the explanation of the rejection, the Examiner has equated the claimed first solder mask to the top mask 90 shown in Figure 9 of the reference. Now, whereas the first solder mask defined in claim 1 of the present Application has first and second areas, with the second area having a thickness less than the thickness of the first area, and associated with the unsheltered portion of the conductive pattern, solder mask 90 only has the claimed first area and

does not have any second area. The same is true for layer 62 of Reed.

Secondly, it follows that solder mask 90 does not have an area that surrounds the base of an unsheltered portion while leaving the tip of that portion exposed. As is clear from Figure 6 of the Application drawing, the second area of the solder mask actually surrounds base 265 of unsheltered portion 263, while tip 266 of the sheltered portion projects upwardly from the base and above the second area of the solder mask.

According to a third distinction, claim 1 specifies that the first solder mask is coated on the top surface of the substrate. A solder mask that is coated on the top surface of a substrate contacts that surface. At no point does solder mask 90 shown in Figure 9 of Reed contact substrate 56.

Finally, application claim 1 specifies that the resin of the first solder mask has a thermal expansion coefficient substantially identical to the thermal expansion coefficient of the resin comprising the substrate. The reference contains no disclosure relating to the coefficient of thermal expansion of any of the components of the printed circuit disclosed therein. In particular, and contrary to the Examiner's assertion, the reference does not contain any

disclosure that substrate 56 and mask 90 are made of the same dialetric material.

The portion of the reference specification on which the Examiner relies to support this assertion, column 3, lines 63-68, discuss the characteristics of the dielectric material of layers 22 and 24, which do not function as solder masks, even though it is disclosed in the reference that they may be made of the type of materials ordinarily used to form solder mask layers. Layers 22 and 24 form substantially continuous insulating layers, and thus perform a function different from that of solder masks. A layer cannot be considered to be a solder mask unless it is used to perform the function of a solder mask. In any event, the reference specification simply describes substrate 16 as a "suitable insulative substrate" and there is simply no indication anywhere in the reference of any particular relation, with respect to any particular property, between the material of substrate 16 and that of layers 22 and 24.

In fact, the statements at column 3, lines 63-68 of the reference indicate that the considerations underlying the choice of dielectric material for layers 22 and 24 are other than coefficient of thermal expansion. When the dielectric material is chosen on the basis of all the considerations disclosed in that portion of the reference, there is no reason

to believe that the end result will be a dielectric layer having the same coefficient of thermal expansion as the substrate.

In any event, to the extent that the rejection is based on the view that the reference discloses that the substrate and solder mask are made of the same dielectric material, the rejection is unsound because the reference does not contain such a disclosure.

Even if the substrate and solder mask were both made of resin, there is no basis for concluding that they would have substantially identical thermal expansion coefficients. Evidence of this can be found in two attached data sheets providing parameters of various epoxy resin materials.

In the data sheet from Mitsubishi Gas Chemical Company, the characteristics of ten different epoxy resins are listed. For each type, three thermal expansion values are listed. These represent the thermal expansion coefficients in three orthogonal directions. The maximum value for each epoxy resin type varies between 35 and 55ppm/°C. The values shown on this sheet are for epoxy resin materials before being caused to undergo a glass transition.

The data sheet from Taiyo America lists values for two types of epoxy resin solder mask materials and lists the coefficient of thermal expansion (CTE) for those materials. The values of 60ppm and 57ppm are those exhibited by the materials before undergoing glass transition.

The data sheets show that the coefficient of thermal expansion of various epoxy resin materials can vary over a range of nearly 2:1 and the coefficients of the various materials listed on these sheets are quite clearly not substantially identical. Furthermore, the attached data sheets relate to only a few exemplary resins. It would be expected that there are other resins having substantially different CTE values.

Accordingly, it is submitted that claim 1 clearly defines a structure that is not disclosed by Reed and it is therefore requested that the rejection of claim 1, as well as the rejections of all of the other claims, which depend from claim 1, be reconsidered and withdrawn, and that claims 1-8 be allowed.

If the above amendment should not now place the application in condition for allowance, the Examiner is invited to call undersigned counsel to resolve any remaining issues.

Respectfully submitted,

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Amendments to the Drawing:

The attached sheet of drawings includes changes to Figure 6. This sheet, which also includes Figures 4 and 5, replaces the original sheet containing Figures 4-6. In Figure 6, reference numerals 401 and 402 have been replaced by numerals 404 and 406, and reference numeral 266 has been added, as required by the Examiner.

Attachment:Replacement Sheet